AMENDMENTS TO THE SPECIFICATION

Please amend the specification by rewriting the following paragraphs as set forth below in marked-up form. Changes to the specification filed in the Preliminary Amendment of April 18, 2005 have been incorporated herewith.

Please amend the paragraph beginning on page 17, line 7 of the original specification, with the following paragraph:

The sense amplifier and data register control circuit 280 outputs a control signal for controlling the sense amplifier 160 and the data register 290 in accordance with an address matching detection signal MTH from the address matching detection circuit 270 and a control signal from ~~an~~ the multiface array timing generation circuit 200.

Please amend the paragraph beginning on page 17, line 18 of the original specification, with the following paragraph:

The column address latency control circuit 170 generates a control signal for controlling a latency time of column accessing in accordance with an address ADR input from the address latch circuit 100 and outputs it to the sense amplifier and data register control circuit ~~150~~ 280 and the MA, LIO MUX control circuit 180.

Please amend the paragraph beginning on page 18, line 6 of the original specification, with the following paragraph:

The multiface array timing generation circuit 200 generates a control signal for controlling an operation timing at the time of memory accessing and outputs it to the row decoder 110, the sense amplifier 160 and the sense amplifier and data register control circuit 280, respectively.

Please amend the paragraph beginning on page 22, line 10 of the original specification, with the following paragraph:

The register equalizer 296 precharges the input side of the data register 290 at a power source voltage V_{DD} before writing. Therefore, the input side of the data register ~~190~~ 290 is kept at a high level and the output side is kept at a low level at this time.

Please amend the paragraph beginning on page 22, line 20 of the original specification, with the following paragraph:

In the sense amplifier bank having the above configuration, retrieving of the write data in the data register 290 is performed as described below. First, a reset signal ~~RESE~~ RESET is activated (kept at a low level), the register equalizer 296 is activated in accordance therewith, and an input terminal of the data register 290 is precharged at a power source voltage V_{DD}. Then, the write signal W2R to the data register is activated (kept at a high level), so that the write gate 298 is opened and the input side of either one of two latch circuits composing the data register 290 is kept at a low level in accordance with the write data input from the write data lines WLIO and WLIOB, and consequently, the write data having inverted logic levels from each other are held in both of the latch circuits composing the data register 290.